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INT CL^6 H01L 21/768 21/8242
Online: WPI, JAPIO, EPODOC

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(54) Abstract Title
A method for forming a self aligned contact in a memory device

(57) A self aligned contact pad in a semiconductor device and a method for forming thereof are disclosed wherein a bit line contact pad ad a storage node contact pad are simultaneously formed with the use of a photoresist layer pattern that has a T shaped opening region including at least two contact regions. The method includes forming an etch stopping layer 106 over a semiconductor substrate 100 ad over a transistor, forming a interlayer dielectric layer 108 over the etch stopping layer 106, the interlayer dielectric layer 108 having a planar top surface, forming a mask pattern 110 over the interlayer dielectric layer 108 as to expose the active region 101 and a part of the inactive region, the mask pattern 110 having a T-shaped opening region 111, sequentially etching the interlayer dielectric layer 108 and etch stopping layer 106 until a top surface of the semiconductor substrate 100 using the mask pattern 110, thereby to form a self aligned contact opening 111a exposing a top surface of the semiconductor substrate 100, removing the mask pattern 110, forming a conductive layer 112 in the self aligned contact opening 111a and over the interlayer dielectric layer 108, and planarization-etching the conductive layer 112 and interlayer dielectric layer 108 until a top surface of the gate mask 104b is exposed, thereby to form at least two contact pads 112a, 112b.

Fig.3G

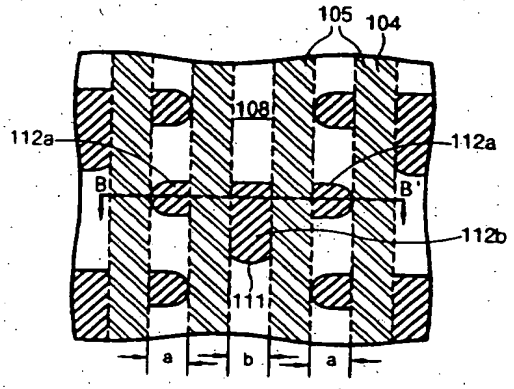

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Fig. 1

(Prior Art)

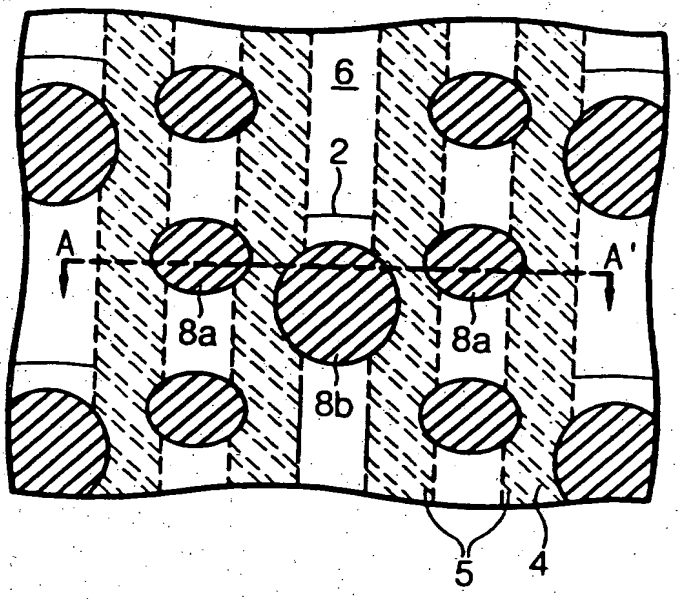


Fig.2A

(Prior Art)

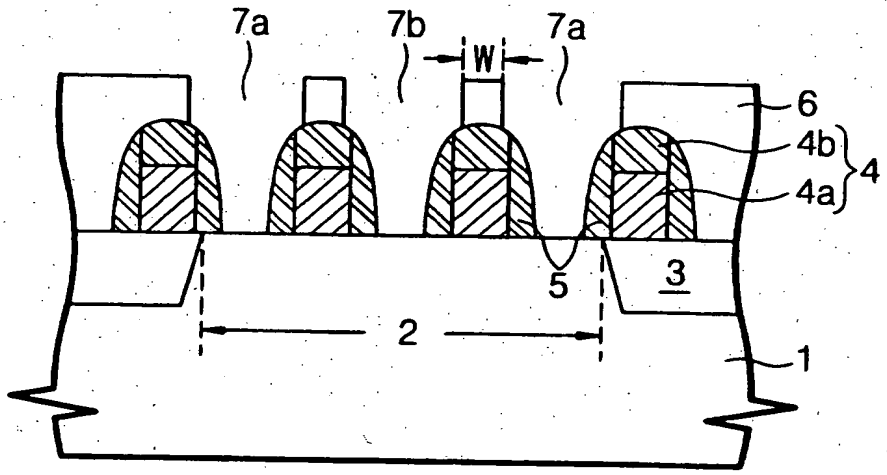


Fig.2B

(Prior Art)

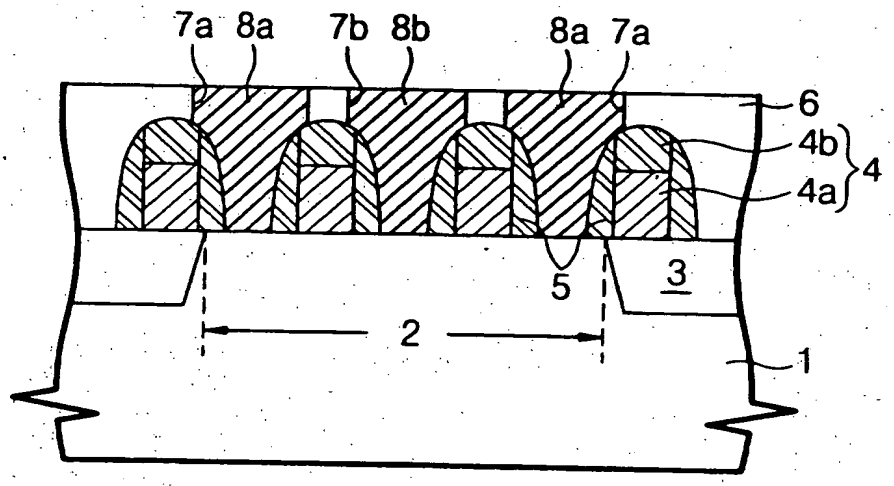


Fig.3A

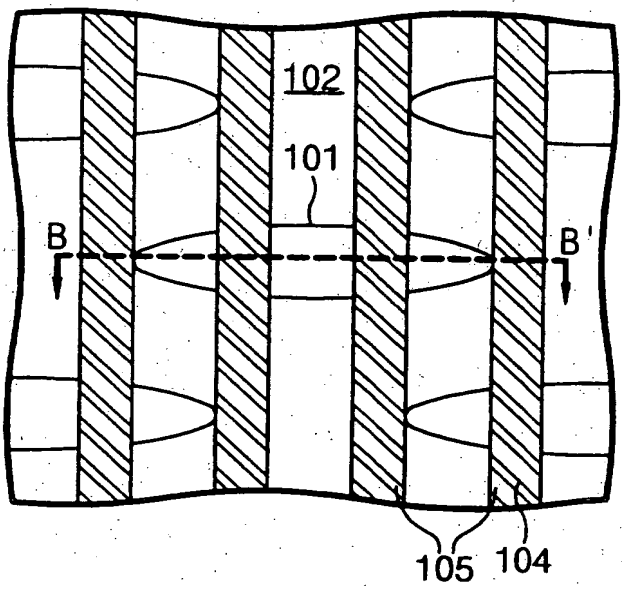


Fig.3B

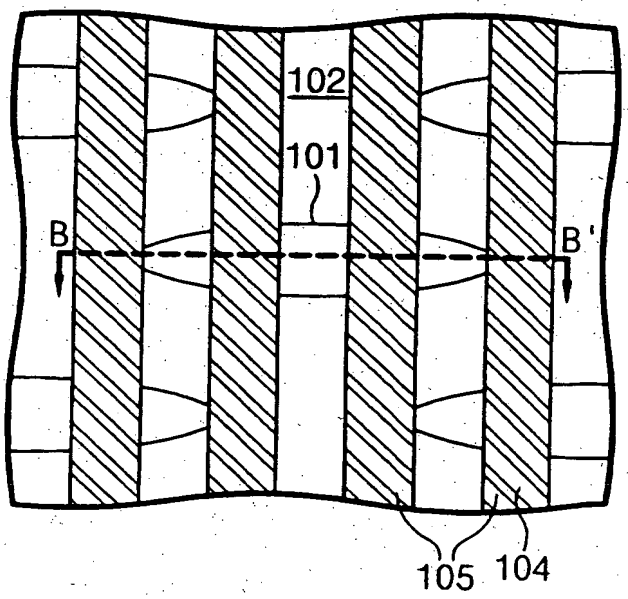


Fig.3C

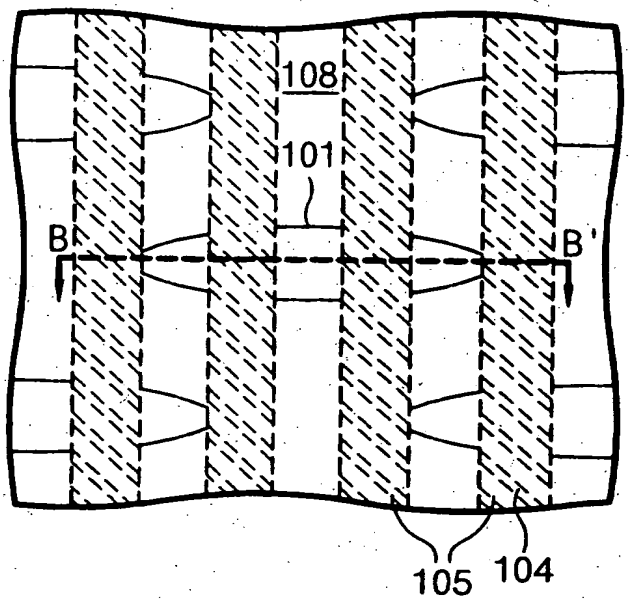


Fig.3D

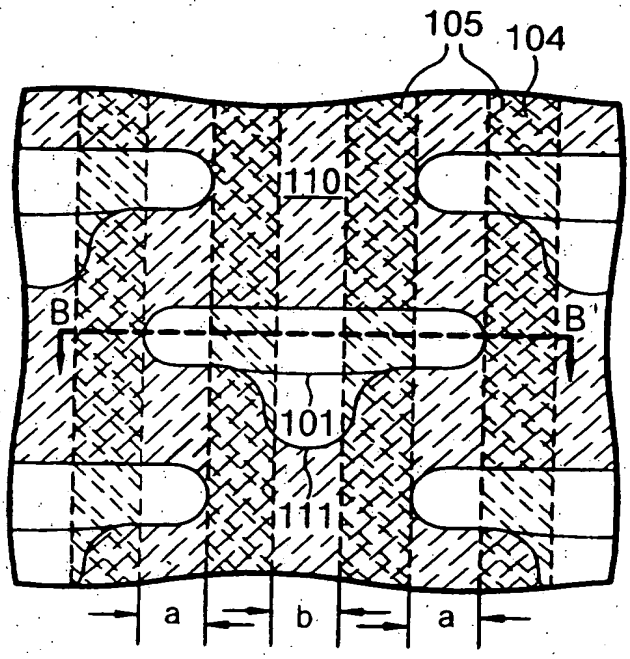


Fig.3E

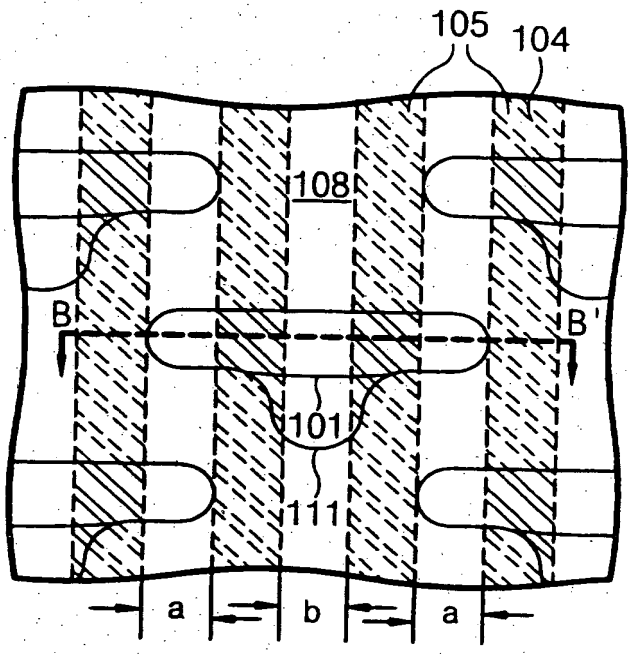


Fig.3F

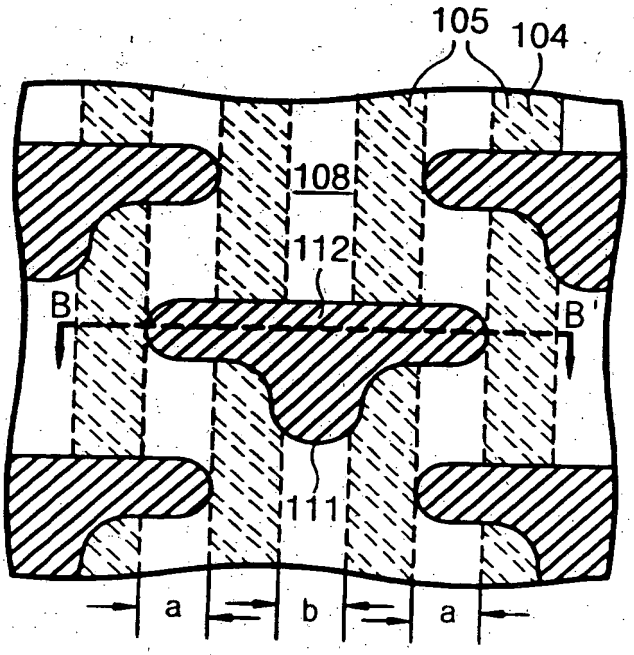


Fig.3G

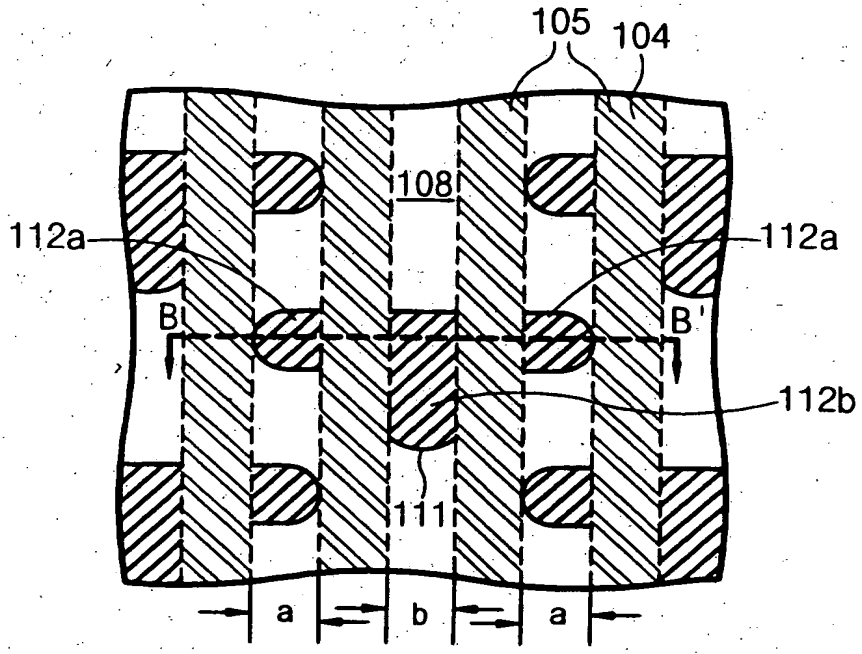


Fig.4A

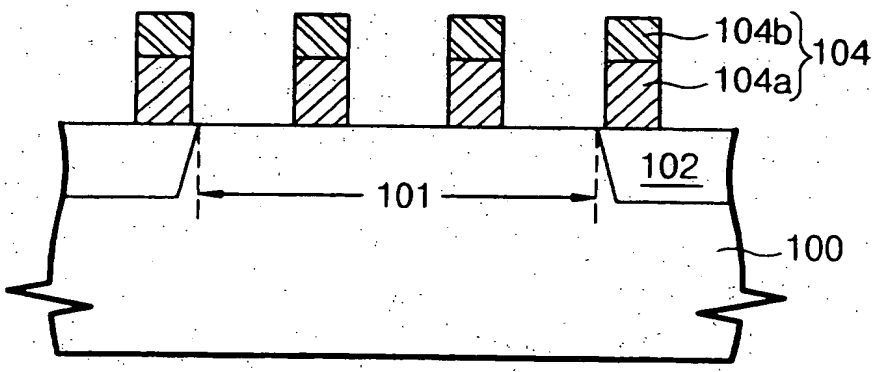


Fig.4B

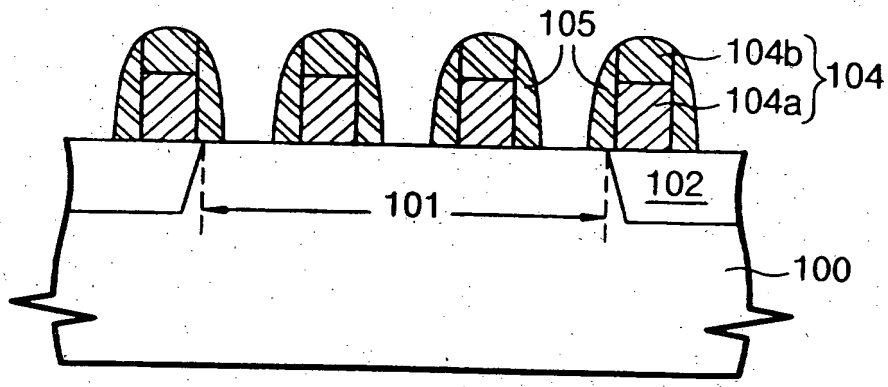

105
104b
104
104a
102
101
100

Fig.4C

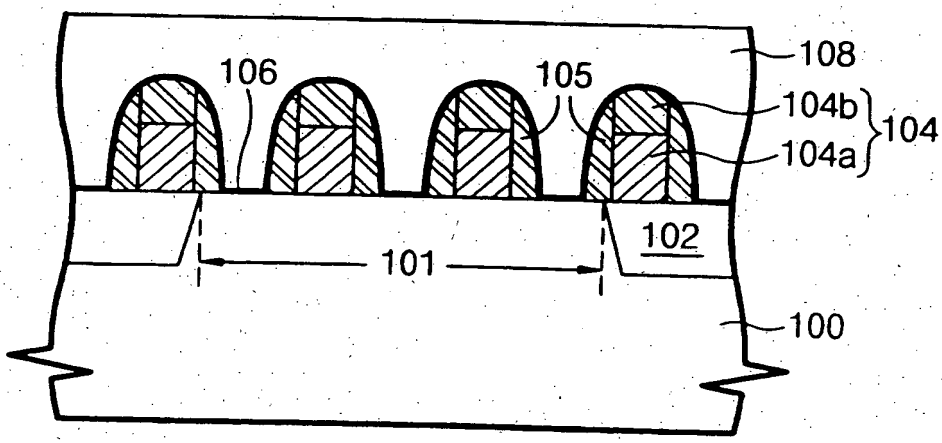

108
106
105
104b
104
104a
102
101
100

Fig.4D

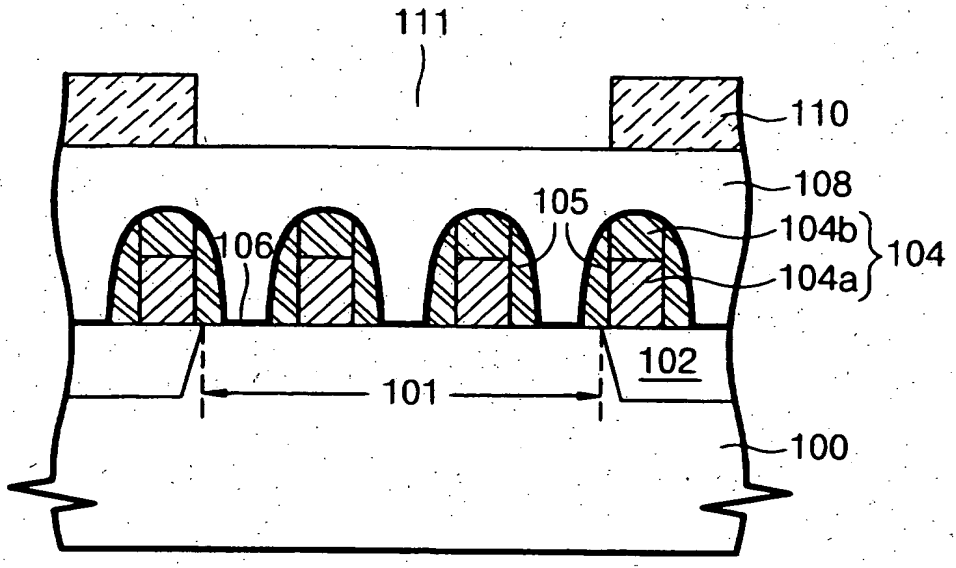

111
110
108
105
104b
104
106
104a
102
101
100

Fig.4E

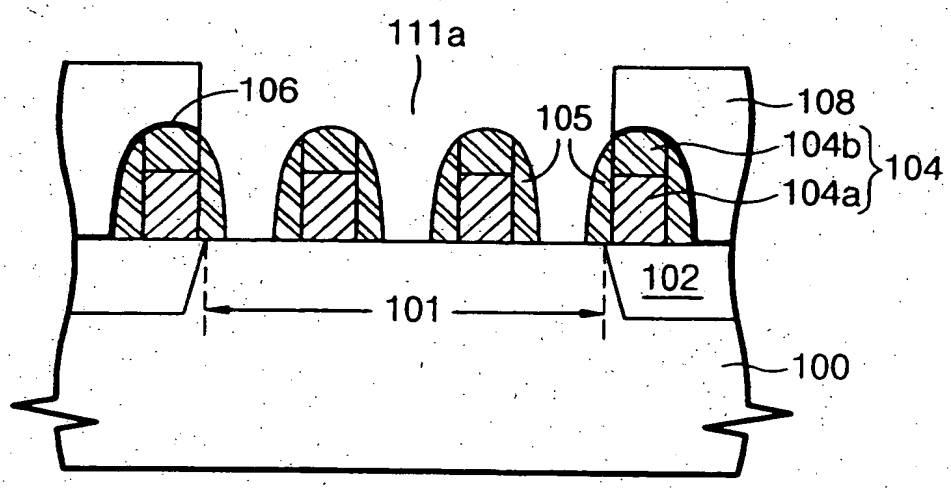

111a
106
108
105
104b
104
104a
102
101
100

Fig.4F

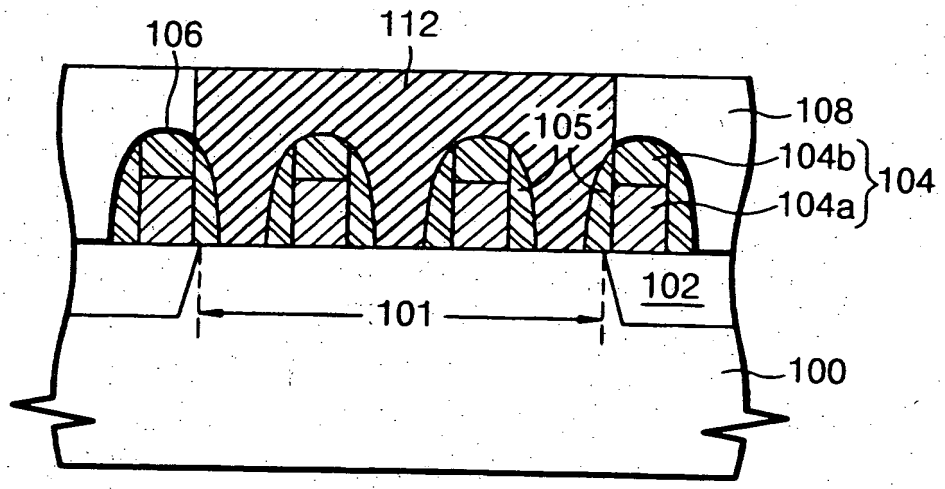

106
112
108
105
104b
104
104a
102
101
100

Fig.4G

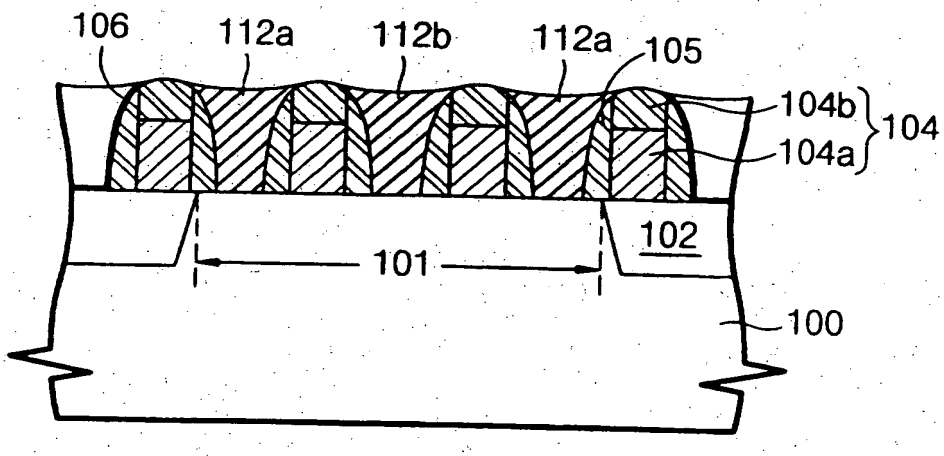

106
112a
112b
112a
105
104b
104
104a
102
101
100

Fig.5A

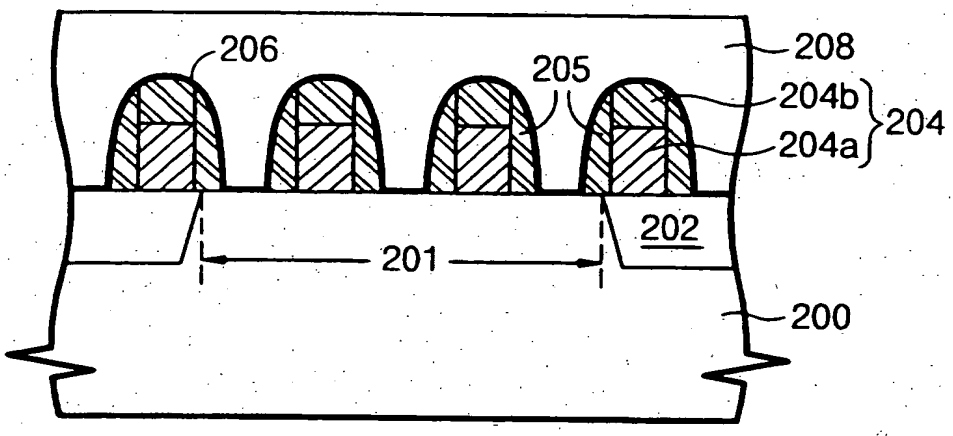

206
205
208
204b
204
204a
202
201
200

Fig.5B

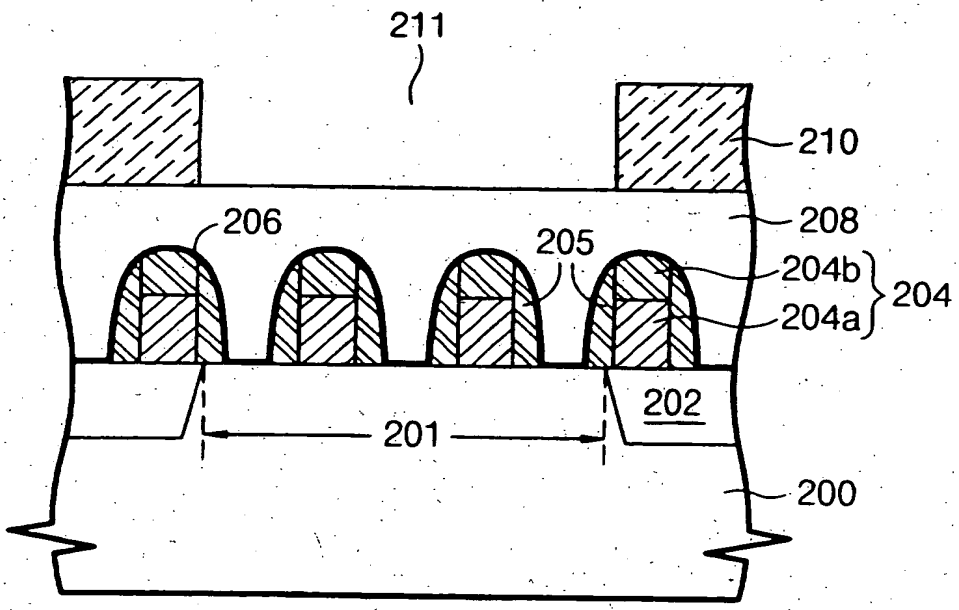

211
210
206
208
205
204b
204
204a
202
201
200

Fig.5C

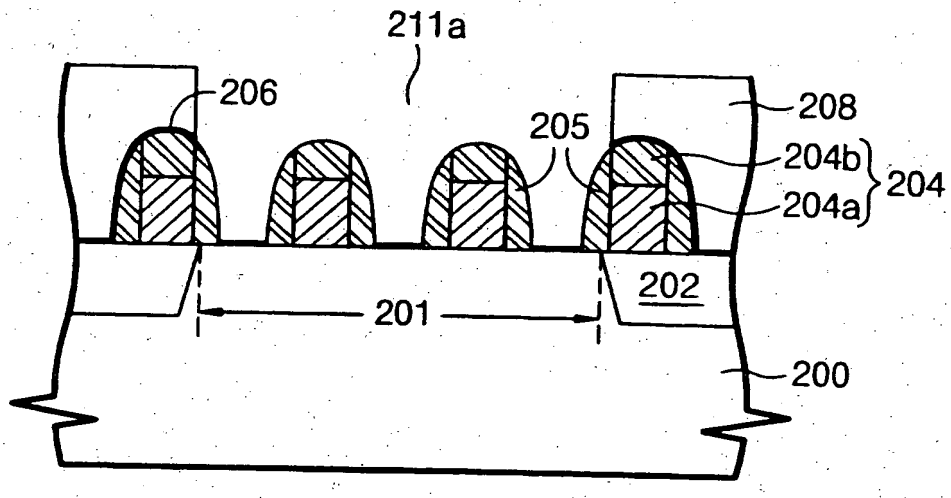

211a
206
208
205
204b
204
204a
202
201
200

Fig.5D

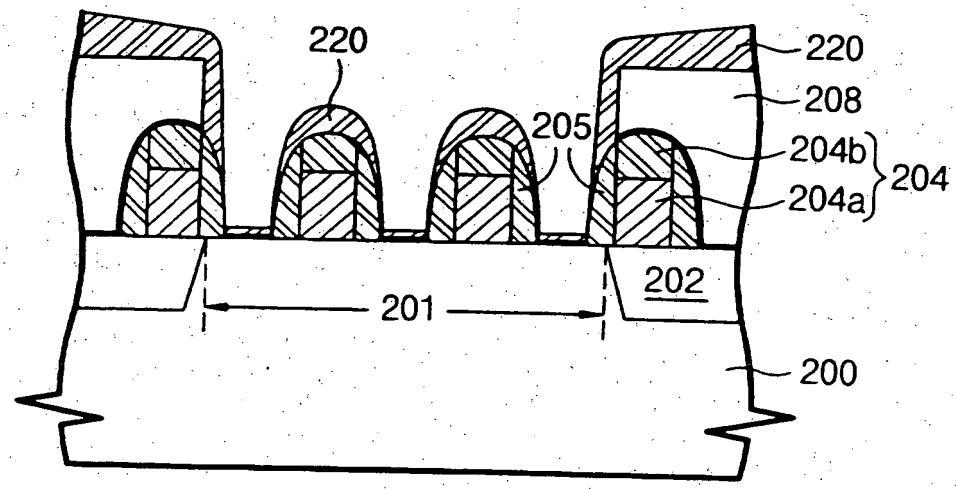
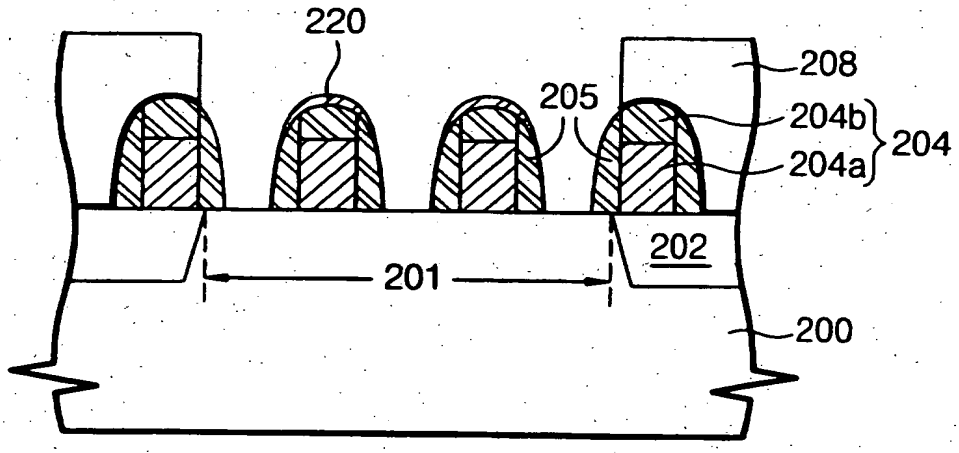

220
220
208
205
204b
204
204a
202
201
200

Fig.5E



A METHOD FOR FORMING A SELF ALIGNED CONTACT IN A SEMICONDUCTOR DEVICE

Field of the Invention

The present invention relates to a contact in a semiconductor device and a method for forming thereof, more particularly to a self aligned contact and a method for forming thereof.

Background of the Invention

Recently, with the advance of semiconductor technique, a trend toward smaller design rules for semiconductor devices such as 1Giga bit DRAMs have proceeded to the extend that alignment margin can hardly be secured when aligning a contact plug with a semiconductor layer or interconnect layer underlying the contact plug. In 1Gbit DRAMs which have design rule of 0.45pitch or less, maximum permissible line space is very small and the size of contacts must be 0.15μm or less, and, thus the formation of a bit contact or a contact for storage node using the conventional direct contact method is not as easy as it appears. Accordingly, for sub-quarter micron semiconductor devices, a manufacturing process is employed which permits the contact plug to be formed by self alignment with a semiconductor layer or interconnect layer underlying the contact plug.

The advantage of the self aligned contact(hereinafter referred to "SAC") is that the misalignment margin can be increased during the step of photolithography and the contact resistance can be reduced. For this reason, emphasis has been place upon the SAC technique in the art.

However, as the pattern size becomes increasingly smaller, there may be a possibility of the short between the contact hole and the gate line. Contact holes of a high integration density device such as a memory device become inevitably a high aspect ratio, that is, a smaller area comparing with the depth. Therefore, etch stop phenomenon occurs during the

step of forming the contact holes.

To solve above-mentioned problems, a method has been proposed which utilizes a contact pad. Hereinafter, the conventional method for forming contact hole using the SAC pad will be described with reference to the Fig.1 to Fig.2.

Fig.1 is a top plan view showing SAC pad structure according to the conventional method and Fig.2A to Fig.2B are flow diagrams showing the process steps of forming the SAC pad which are cross-sectional views taken along A-A′ line of Fig.1.

First, referring to Fig.2A, a device isolation region 3 is formed over a semiconductor substrate 1 to define active 2 and inactive regions. The device isolation region 3 may be formed by any suitable method well known in the art, for example, shallow trench isolation(STI) and local oxidation of silicon(LOCOS). A gate oxide layer(not shown) is formed by a conventional method, i.e., thermal oxidation method and a gate electrode conductive layer and a gate mask insulating layer are laminated over the gate oxide layer in this order. The gate electrode conductive layer is generally laminated with polysilicon and tungsten silicide and the gate mask insulating layer is made of a silicon nitride(SiN) layer or silicon oxynitirde(SiON) layer which has an etch selectivity ratio with respect to subsequent interlayer dielectric layer 6. The photolithography well known in the art is conducted on the electrode conductive layer and the gate mask layer to thereby form a gate electrode structure 4, i.e., gate mask layer 4b and gate electrode 4a.

Low concentration impurity ions are implanted into the active region 2 of the semiconductor substrate 1 both outside of the gate electrode structure 4 so as to form low concentration source/drain region for LDD(lightly doped drain) structure. A gate spacer 5 is formed on sidewalls of the gate electrode structure 4. The gate spacer 5 also has an etch selectivity ratio with respect to the subsequent interlayer dielectric layer 6 and formed of generally silicon nitride or silicon oxynitride layer. Thereafter, high concentration impurity ions are implanted into the active region 2 of the semiconductor substrate 1 both outside of the gate spacer 5 so as to form high concentration source/drain region and thereby forming a transistor having the LDD structure.

The interlayer dielectric layer 6 is deposited over the semiconductor substrate 1 and a photoresist pattern(not shown) for self aligned contact is deposited over the interlayer dielectric layer 6. The interlayer insulating film 6 is etched by using the photoresist pattern as a mask thereby to form contact holes 7a and 7b.

Referring to Fig.2B, the photoresist pattern is removed and the contact holes 7a and 7b are filled up with a conductive material layer such as a polysilicon. The polysilicon layer is then planarized by such as CMP(chemical mechanical polish) or etch-back thereby to form self aligned contact pads 8a and 8b, i.e., bit line contact pad 8b and storage node contact pad 8a are respectively formed. In high density device which has design rule of 0.45pitch or less, it can be very difficult to perform the photolithography so as to form the contact holes 7a and 7b which must be horizontally electrically isolated by the interlayer dielectric layer 6 having very narrow width size "W" shown in Fig.2A.

In such conventional method for forming the SAC pad, the self aligned contact pattern is circle type or ellipse type, as shown in Fig.1, i.e., the photoresist pattern has an opening such circle type or ellipse type. Therefore as the device pattern size becomes smaller, i.e., as the aspect ratio of the contact hole becomes high, the area which is to be etched reduces and the depth of the contact hole increases. As a result, during the step of etching the interlayer insulating film, the etching rate becomes reduced and the reaction byproduct cannot diffuse out of the contact hole in severe case, so that the etching rate is significantly reduced and etching is ceased, i.e., etch stop phenomenon occurs.

To solve the etch stop phenomenon, the etching must be performed under the condition that formation of the byproduct such as polymer is suppressed and the etching time must be increased. However, in case of such etching condition, the gate mask layer and sidewall gate spacer is etched during the etching step, thereby resulting in short between the SAC pad and gate.

For the purpose of solving above problems, Y.Kohyama et al, has proposed a method for forming SAC pad which utilizes the contact pattern merging storage node contact hole and bit line contact hole in the article entitled " A Fully Printable, Self-aligned and

Planarized Stacked Capacitor DRAM Cell Technology for 1Gbit DRAM and Beyond", symp, on VLSI tech, digest of technical papers, pp. 17-18, 1997.

In this invention, the gate SAC pattern(which indicates resist area) is the same as active area and is shifted by a half pitch to gate direction. Therefore, the photoresist pattern area is so small that the polymer formation is very low during the step of forming the contact hole. As a result, the etch selectivity ratio the interlayer insulating film to the nitride layer of gate spacer and gate mask layer becomes low. This is because the polymer formation is proportion to the photoresist pattern area and the etching selectivity ratio increases with polymer formation.

Summary of the Invention

The present invention provides an improved method for forming a self aligned contact in a semiconductor substrate. A key feature of the invention is forming self aligned contact mask which exposes active region and a part of inactive region through T shaped opening.

Accordingly, an object of the present invention is to provide a self aligned contact and a method for forming thereof which prevent the etch stop phenomenon.

It is another object of the invention to provide a fully printable a self aligned contact.

It is yet another object of the invention to provide a method for forming a self aligned contact which has a good etch selectivity ratio during the step of etching self aligned contact.

Other aspect, objects, and the several advantages of the present invention will be apparent to one skilled in the art from a reading of the following disclosure and appended claims.

To achieve these and other advantages and in accordance with the purpose of the present invention, the method for forming the self aligned contact in a semiconductor device includes forming a gate stack spaced apart from each other over a semiconductor. The gate stack consists of a gate electrode, a gate mask of nitride layer formed thereon, and a sidewall gate spacer of nitride layer. As is well known, gate oxide layer has been formed between

the gate electrode and the semiconductor substrate, and an active region and inactive region are defined by a field oxide layer over the semiconductor substrate. An etch stopping layer against SAC etch is formed in space between gate stacks and over gate stack to a thickness of about 100Å. The etch stopping layer is made of insulating material such as nitride layer which has an etch selectivity ratio to subsequent an interlayer dielectric layer of oxide layer. The interlayer dielectric layer is formed over the etch stopping layer to a thickness of about 3000Å to 9000Å to sufficiently cover the gate stack. The interlayer dielectric layer is then planarize to increase photolithography process margin. Alternatively, the planarization process is performed down to a top surface of the gate stack and then another interlayer dielectric layer is formed over the resulting structure to a predetermined thickness.

The next process sequence is critical to this invention. A mask pattern preferably made of photoresist layer is so formed over the planar interlayer dielectric layer as to expose an active region and a part of an inactive region and the mask pattern has a T-shaped opening region. Namely, the mask pattern exposes bit line contact region and storage node contact region through one opening. Accordingly, the etch stop phenomenon encountered in the prior art method can be avoided since the opening region by the mask pattern is relatively large. On the other hand, the opening region is relatively small compared with that of Y.Kohyama et al, so that the selectivity etch for self aligned contact is good.

The interlayer dielectric layer and etch stopping layer is etched using the mask pattern, thereby to form a self aligned contact opening which expose a top surface of the semiconductor substrate between gate stacks. After the mask pattern is removed by conventional method, a conductive layer preferably made of a polysilicon layer is formed in the self aligned contact opening and over the interlayer dielectric layer to a thickness of about 3000Å to 7000Å. Planarization-etching such as CMP or etch-back is performed on the conductive layer and interlayer dielectric layer until a top surface of the gate stack, i.e., gate mask of nitride layer is exposed, thereby to form contact pads, i.e., form respectively bit line contact pad and storage node contact pad.

In the etching step of forming the self aligned contact opening, the gate mask may be

lost and thus there is a possibility of poly stringer formation. Therefore, wet etch or dry etch can be further performed on a top surface of the contact pads so as to remove the poly stringer and thereby preventing a bridge between the bit line contact pad and storage node contact pad. The wet etch may use SC1(a mixture of NH_3, H_2O_2, and deionized water) and the dry etch may use chlorine-based gas chemistry.

In another embodiment of the invention, the method includes forming a gate stack spaced apart from each other over a semiconductor. The gate stack consists of a gate electrode, a gate mask of nitride layer formed thereon, and a sidewall gate spacer of nitride layer. As is well known, gate oxide layer has been formed between the gate electrode and the semiconductor substrate, and an active region and inactive region are defined by a field oxide layer over the semiconductor substrate. An etch stopping layer against SAC etch is formed in space between gate stacks and over gate stack to a thickness of about 100Å. The etch stopping layer is made of insulating material such as nitride layer which has an etch selectivity ratio to subsequent an interlayer dielectric layer of oxide layer. The interlayer dielectric layer is formed over the etch stopping layer to a thickness of about 3000Å to 9000Å to sufficiently cover the gate stack. The interlayer dielectric layer is then planarize to increase photolithography process margin. Alternatively, the planarization process is performed down to a top surface of the gate stack and then another interlayer dielectric layer is formed over the resulting structure to a predetermined thickness.

A mask pattern preferably made of photoresist layer is so formed over the planar interlayer dielectric layer as to expose an active region and a part of an inactive region and the mask pattern has a T-shaped opening region. Namely, the mask pattern exposes bit line contact region and storage node contact region through one opening. Accordingly, the etch stop phenomenon encountered in the prior art method can be avoided since the opening region by the mask pattern is relatively large. On the other hand, the opening region is relatively small compared with that of Y.Kohyama et al, so that the selectivity etch for self aligned contact is good.

The interlayer dielectric layer is etched using the mask pattern until the etch stopping

layer between the stack gates is exposed. After that, the mask pattern is removed. The next process sequence is critical to this method. A material layer made of nitride layer is deposited over the resulting structure. The deposition of the material layer is so conducted as to have a poor step coverage. Namely, the material layer is deposited a larger amount on the interlayer dielectric layer and a top surface of the gate stack than the bottom portion between the gate stacks, i.e., on the etch stopping layer. The material layer is deposited to have a thickness of about 200Å to 1500Å and PECVD(plasma enhanced chemical vapor deposition) technique can be used to provide intentionally a poor step coverage. This material layer is provided to compensate the loss of the gate mask during the step of etching the etch stopping layer between the gate stacks thereby minimizing the step between the gate stacks.

After that, the material layer and the etch stopping layer between the gate stacks are etched back thereby to form a self aligned contact opening.

A conductive layer preferably made of a polysilicon layer is formed in the self aligned contact opening and over the interlayer dielectric layer to a thickness of about 3000Å to 7000Å. Planarization-etching such as CMP or etch-back is performed on the conductive layer and interlayer dielectric layer until a top surface of the gate stack, i.e., gate mask of nitride layer is exposed, thereby to form contact pads, i.e., form respectively bit line contact pad and storage node contact pad.

In the etching step of forming the self aligned contact opening, the gate mask may be lost and thus there is a possibility of poly stringer formation. Therefore, wet etch or dry etch can be further performed on a top surface of the contact pads so as to remove the poly stringer and thereby preventing a bridge between the bit line contact pad and storage node contact pad. The wet etch may use SC1(a mixture of NH_3, H_2O_2, and deionized water) and the dry etch may use chlorine-based gas chemistry.

Brief Description of the Drawings

The invention may be understood and its objects will become apparent to those

skilled in the art by reference to the accompanying drawings as follows:

Fig.1 is a top plan view showing SAC pad structure according to the conventional method;

Fig.2A to Fig.2B are flow diagrams showing the process steps of forming the self aligned contact which are cross-sectional views taken along A-A′ line of Fig.1;

Fig.3A to Fig.3G are top plan views showing the process steps of a novel method for forming a self aligned contact according to one embodiment of the present invention;

Fig.4A to Fig.4G are flow diagrams showing the process steps of forming the self aligned contact which are cross-sectional views respectively taken along B-B′ line of Fig.3A to Fig.3G; and

Fig.5A to Fig.5E are flow diagrams showing the process steps of forming the self aligned contact according to another embodiment of the present invention.

Detailed Description of the Preferred Embodiments

The preferred embodiment of the present invention will now be described with reference to the accompanying drawings, Fig.3 to Fig.5. In Fig.4A to Fig.4G, the same parts function as shown in Fig.3A to Fig.3G are identified with same reference numbers.

Fig.3A to Fig.3G are top plan views showing the process steps of a novel method for forming a self aligned contact according to one embodiment of the present invention and Fig.4A to Fig.4G are flow diagrams showing the process steps of forming the self aligned contact which are cross-sectional views respectively taken along B-B′ line of Fig.3A to Fig.3G. First, referring to Fig.3A and Fig.4A, a device isolation region 102, i.e., field oxide layer is formed on the predetermined region of a semiconductor substrate 100 to define an active region 101 and an inactive region. The device isolation region 102 may be formed by any suitable method well known in the art, for example shallow trench isolation(STI) and local oxidation of silicon(LOCOS). The active region 101 is formed to have a longitudinal ellipse shaped configuration from the top plan view. A gate oxide layer(not shown) is

formed by conventional method. A gate electrode conductive layer and gate mask insulating layer are laminated over the gate oxide layer. The gate electrode conductive layer is generally formed of polysilicon layer or laminated with polysilicon and silicide layers to have a thickness of about 2000Å. The gate mask layer is formed of material layer which has an etch selectivity ratio to subsequent interlayer dielectric layer 108. The gate mask layer is formed of silicon nitride layer(SiN) or silicon oxynitride layer(SiON) and has a thickness of about 1000Å to 2000Å.

The photolithography well known in the art is conducted on the electrode conductive layer and the gate mask layer thereby to form gate electrode structure line 104, i.e., gate mask layer 104b and gate electrode 104a. Herein, pass gate is formed to have a curved part along edge of the active region so as to increase space between the gate thereby increasing process margin of self aligned contact etch and decreasing contact not opening.

Low concentration impurity ions are implanted into the active region in the semiconductor substrate 100 both outside of the gate electrode structure 104 thereby to form low concentration source/drain region for LDD(lightly doped drain) structure.

Referring to Fig.3B and Fig.4B, an insulating layer for a gate spacer 105 is formed to have a thickness of about 500Å to 1000Å and etched back to form the gate spacer 105 on both lateral sidewalls of the gate electrode structure 104. Herein, the gate spacer 105 also has etch selectivity ratio with respect to the subsequent interlayer dielectric layer 108 and formed of silicon nitride and silicon oxynitride layer. Thereafter, high concentration impurity ions are implanted into the active region in the semiconductor substrate 100 both outside of the gate spacer 105 so as to form high concentration source/drain region thereby forming a transistor having the LDD structure.

Referring to Fig.3C and Fig.4C, a thin layer of etch stopping layer 106 against subsequent self aligned contact etch is formed over the semiconductor substrate 100 including the transistor to a thickness of about 100Å. The etch stopping layer 106 formed of nitride layer such as silicon nitride layer or silicon oxynitride layer which has an etch

selectivity ratio to the interlayer dielectric layer 108. The interlayer dielectric layer 108 is then deposited to a thickness about 3000Å to 9000Å sufficient to cover the transistor. The interlayer dielectric layer may be formed of high density plasma(HDP) chemical vapor deposition(CVD) oxide layer which has good filling characteristics without void formation therein. The interlayer dielectric layer is then planarized to improve photolithography process margin. The planarization process may use CMP(chemical mechanical polishing) or etch back and is so performed down to the interlayer dielectric layer 108 as to have a thick of about 500Å to 1000Å from the top surface of the transistor, i.e., gate mask 104b.

Alternatively, the planarization may be performed down to the top surface of the gate mask 104b. In this case, another interlayer dielectric layer is redeposited to have a predetermined thickness, i.e., about 500Å to 1000Å.

The next process sequence is critical to this invention. Referring to Fig.4d, a mask pattern 110 preferably made of photoresist is formed over the planar interlayer dielectric layer 108. The photoresist pattern 110 is formed to have a T shaped opening region 111 which exposes the active region 101 and a part of the inactive region, as shown in Fig.3D. Namely, the T shaped opening region 111 exposes simultaneously bit line contact region(b) and storage node contact region(a). Accordingly, the etch stop phenomenon encountered in the prior art method(which has a circle or ellipse shaped opening as illustrated in Fig.1) can be avoided since the opening region by the mask pattern is relatively large. On the other hand, the opening region is relatively small compared with that of Y.Kohyama et al, so that the selectivity etch for self aligned contact is good.

In Fig.3E and Fig.4E, the interlayer dielectric layer 108 is etched using the photoresist pattern 110 as a mask. Herein, the self aligned contact is opened by etching the interlayer dielectric layer 108 selectively to each of the gate mask 104b, sidewall gate spacer 105, and the etch stopping layer 106. Then, the etch stopping layer 106 between the transistors is removed thereby to form a self aligned contact opening 111a which exposes the semiconductor substrate 100 between the transistors, i.e., the bit line contact region(b) and

storage node contact region(a).

After removing the photoresist pattern 110, a conductive layer 112 as for self aligned contact pad such as polysilicon layer is deposited in the self aligned contact opening 111a and over the interlayer dielectric layer 108. The conductive layer 112 is formed to have a thickness of about 3000Å to 7000Å. The planarization process such as CMP or etch-back is performed until a top surface of the interlayer dielectric layer 108 is exposed, as shown in Fig.3F and Fig.4F. In case of the CMP, slurry is used for polysilicon layer etching.

Finally, the interlayer dielectric layer 108 and the polysilicon layer 112 are planarized by CMP and the self aligned bit line contact pad 112b and storage node contact pad 112a are formed, as shown in Fig.3G and Fig.4G. The CMP uses a slurry for oxide layer etching.

In the etching step of forming the self aligned contact opening 111a, the gate mask 104b may be lost and thus there is a possibility of poly stringer formation. Therefore, wet etch or dry etch can be further performed on a top surface of the contact pads 112a and 112b so as to remove the poly stringer and thereby preventing a bridge between the bit line contact pad 112b and storage node contact pad 112a. The wet etch may use SC1(a mixture of NH_3, H_2O_2, and deionized water) and the dry etch may use chlorine-based gas chemistry.

Practically, if the step of forming the self aligned contact opening is performed right after the planarization process is performed down to the top surface of the gate mask, about 500Å to 900Å of gate mask is etched and thereby causing the step between the transistors. This makes it difficult to remove the poly stringer during the step of the wet or dry etching the contact pads.

However, as described above, according to this invention, the planarization process so performed that the interlayer dielectric layer 108 has a thickness of about 500Å to 1000Å from the top surface of the gate mask 104b. If the planarization process is performed down to the top surface of the gate mask 104b, another interlayer dielectric layer is formed thereon to a thickness of about 500Å to 1000Å. Therefore, in accordance with the present invention, only a small amount of the gate mask 104b about 200Å is etched during the step of forming

the self aligned contact opening 111a. Therefore, the good characteristics of contact pads without the poly stringer can be obtained.

Fig.5A to Fig.5E are flow diagrams showing the process steps of forming the self aligned contact according to another embodiment of the present invention.

Referring to Fig.5A, a device isolation region 202, i.e., field oxide layer is formed on the predetermined region of a semiconductor substrate 200 to define an active region 201 and an inactive region. The device isolation region 202 may be formed by any suitable method well known in the art, for example shallow trench isolation(STI) and local oxidation of silicon(LOCOS). The active region 201 is formed to have a longitudinal ellipse shaped configuration from the top plan view. A gate oxide layer(not shown) is formed by conventional method. A gate electrode conductive layer and gate mask insulating layer are laminated over the gate oxide layer. The gate electrode conductive layer is generally formed of polysilicon layer or laminated with polysilicon and silicide layers to have a thickness of about 2000Å. The gate mask layer is formed of material layer which has an etch selectivity ratio to subsequent interlayer dielectric layer 208. The gate mask layer is formed of silicon nitride layer(SiN) or silicon oxynitride layer(SiON) and has a thickness of about 1000Å to 2000Å.

The photolithography well known in the art is conducted on the electrode conductive layer and the gate mask layer thereby to form gate electrode structure line 204, i.e., gate mask layer 104b and gate electrode 204a. Herein, pass gate is formed to have a curved part along edge of the active region so as to increase space between the gate thereby increasing process margin of self aligned contact etch and decreasing contact not opening. Low concentration impurity ions are implanted into the active region in the semiconductor substrate 200 both outside of the gate electrode structure 104 thereby to form low concentration source/drain region for LDD(lightly doped drain) structure. An insulating layer for a gate spacer 205 is formed to have a thickness of about 500Å to 1000Å and etched back to form the gate spacer 205 on both lateral sidewalls of the gate electrode structure 104. Herein, the gate spacer 205

also has etch selectivity ratio with respect to the subsequent interlayer dielectric layer 208 and formed of silicon nitride and silicon oxynitride layer. Thereafter, high concentration impurity ions are implanted into the active region in the semiconductor substrate 200 both outside of the gate spacer 205 so as to form high concentration source/drain region thereby forming a transistor having the LDD structure.

A thin layer of etch stopping layer 206 against subsequent self aligned contact etch is formed over the semiconductor substrate 200 including the transistor to a thickness of about 100Å. The etch stopping layer 206 formed of nitride layer such as silicon nitride layer or silicon oxynitride layer which has an etch selectivity ratio to the interlayer dielectric layer 208. The interlayer dielectric layer 208 is then deposited to a thickness about 3000Å to 9000Å sufficient to cover the transistor. The interlayer dielectric layer may be formed of high density plasma(HDP) chemical vapor deposition(CVD) oxide layer which has good filling characteristics without void formation therein. The interlayer dielectric layer 208 is then planarized to improve photolithography process margin. The planarization process may use CMP(chemical mechanical polishing) or etch back and is so performed down to the interlayer dielectric layer 108 as to have a thick of about 500Å to 1000Å from the top surface of the transistor, i.e., gate mask 204b.

Alternatively, the planarization may be performed down to the top surface of the gate mask 204b. In this case, another interlayer dielectric layer is redeposited to have a predetermined thickness, i.e., about 500Å to 1000Å.

Referring to Fig.5B, a mask pattern 210 preferably made of photoresist is formed over the planar interlayer dielectric layer 208. The photoresist pattern 210 is formed to have a T shaped opening region 211 which exposes the active region 201 and a part of the inactive region, as illustrated in Fig.4D. Namely, the T shaped opening region 211 exposes simultaneously bit line contact region and storage node contact region. Accordingly, the etch stop phenomenon encountered in the prior art method(which has a circle or ellipse shaped opening as illustrated in Fig.1) can be avoided since the opening region by the mask

pattern is relatively large. On the other hand, the opening region is relatively small compared with that of Y.Kohyama et al, so that the selectivity etch for self aligned contact is good.

Referring to Fig.5C, the interlayer dielectric layer 208 is etched using the photoresist pattern 210 as a mask and thereby forming a self aligned contact opening 211a. The self aligned contact is opened by etching the interlayer dielectric layer 208 selectively to each of the gate mask 204b, sidewall gate spacer 205, and the etch stopping layer 206. During this self aligned etching step, the top surface of the transistor, i.e., the gate mask 104b may be etched because the step between the top surface of the transistor and bottom part adjacent to the transistor. Accordingly, a larger amount of insulating layer is etched on the top part of the transistor than the bottom part adjacent to the transistor. This may result in difference in the height of the transistor and thereby make it difficult to perform planarization of subsequent conductive layer.

For this reason, a material layer 220 to compensate the loss of the gate mask 104b is deposited over the resulting structure, as shown in Fig.5D. Therefore, the compensation mask layer 220 must be deposited a larger amount on a top part of the transistor and the interlayer dielectric layer 208 than bottom space adjacent to the transistor. For this object, the silicon nitride layer or silicon oxynitride layer may be deposited by plasma enhanced chemical vapor deposition. The compensation mask 220 is deposited to have a thickness of about 200Å to 1500Å.

After that, as shown in Fig.5E, the etch stopping layer 206 and the compensation mask layer 220 are removed by etch back process and thereby to expose bit line contact region and storage node contact region between the transistors. The next process sequences are the same as the first embodiment illustrated in Fig4F to Fig.4G. Namely, a conductive layer(not shown) as for self aligned contact pad such as polysilicon layer is deposited in the self aligned contact opening 211a and over the interlayer dielectric layer 208. The conductive layer is formed to have a thickness of about 3000Å to 7000Å. The planarization

process such as CMP or etch-back is performed until a top surface of the interlayer dielectric layer 208 is exposed. In case of the CMP, slurry is used for polysilicon layer etching.

Finally, the interlayer dielectric layer 208 and the polysilicon layer are planarized by CMP and the self aligned bit line contact pad and storage node contact pad are formed. The CMP uses a slurry for oxide layer etching.

As understood from the explanation, in accordance with the present invention, a bit line contact region and a storage node contact region are simultaneously exposed with the use of a photoresist layer pattern that has a T shaped opening region. Therefore the etch stop phenomenon can be avoided and the etch selectivity of the interlayer dielectric layer to the gate mask and spacer can be improved. Further fully printable the self aligned contact pads are formed with good reliability.

While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of this invention.

What is claimed is:

1. A method for forming a self aligned contact in a semiconductor device having a semiconductor substrate, a device isolation layer formed on said semiconductor substrate to define active and inactive regions, and a transistor formed on said active and inactive regions, said transistor being formed of a gate electrode, a gate mask thereon, and a sidewall gate spacer, said method comprising the steps of:

forming an etch stopping layer over said semiconductor substrate and over said transistor;

forming an interlayer dielectric layer over said etch stopping layer, said interlayer dielectric layer having a planar top surface;

forming a mask pattern over said interlayer dielectric layer as to expose said active region and a part of said inactive region, said mask pattern having a T-shaped opening region;

sequentially etching said interlayer dielectric layer and etch stopping layer using said mask pattern, thereby to form a self aligned contact opening exposing a top surface of said semiconductor substrate;

removing said mask pattern;

forming a conductive layer in said self aligned contact opening and over said interlayer dielectric layer; and

planarization-etching said conductive layer and interlayer dielectric layer until a top surface of said gate mask is exposed, thereby to form at least two contact pads.

2. The method according to claim 1, wherein each of said gate mask, sidewall gate spacer and etch stopping layer is made of an insulating material having an etch selectivity ratio to said interlayer dielectric layer.

3. The method according to claim 2, wherein said insulating material is made of one selected from a group consisting of SiN and SiON.

4. The method according to claim 1 or 2, wherein said gate mask has a thickness in the range of about 1000Å to 2000Å, said sidewall gate spacer has a thickness in the range of about 500Å to 1000Å, and said etch stopping layer has a thickness of about 100Å.

5. The method according to claim 1, wherein each of said gate mask, sidewall gate spacer and etch stopping layer serves as an etch stopping layer during said step of etching interlayer dielectric layer.

6. The method according to claim 1, wherein said interlayer dielectric layer has a thickness in the range of about 3000Å to 9000Å, and said conductive layer has a thickness in the range of about 3000Å to 7000Å.

7. The method according to claim 1, wherein said T-shaped opening region is a merged contact region including at least two contact regions.

8. The method according to claim 1, wherein said step of planarization-etching is performed by one selected from a group consisting of CMP process, etch-back process, and a combination thereof.

9. The method according to claim 1, further comprises etching, after said step of planarization-etching, a top surface portion of said contact pads.

10. The method according to claim 9, wherein said step of etching a top surface portion of said contact pads is performed by one selected from a group consisting of wet etch

and dry etch processes so as to remove a conductive stringer between said contact pads.

11. A method for forming a self aligned contact in a semiconductor device having a semiconductor substrate, a device isolation layer formed on said semiconductor substrate to define active and inactive regions, and a transistor formed on said active and inactive regions, said transistor being formed of a gate electrode, a gate mask thereon, and a sidewall gate spacer, said method comprising the steps of:

forming an etch stopping layer over said semiconductor substrate and over said transistor;

forming a first interlayer dielectric layer over said etch stopping layer;

planarization-etching said first interlayer dielectric layer until a top surface of said gate mask is exposed;

forming a second interlayer dielectric layer over said first interlayer dielectric layer;

forming a mask pattern over said second interlayer dielectric layer as to expose said active region and a part of said inactive region, said mask pattern having a T-shaped opening region;

sequentially etching said second interlayer dielectric layer, said first interlayer dielectric layer, and said etch stopping layer using said mask pattern, thereby to form a self aligned contact opening exposing a top surface of said semiconductor substrate;

removing the mask pattern;

forming a conductive layer in said self aligned contact opening and over said second interlayer dielectric layer; and

planarization-etching said conductive layer and second interlayer dielectric layer until a top surface of said gate mask is exposed, thereby to form at least two contact pads.

12. The method according to claim 11, further comprises etching, after said step of planarization-etching said conductive layer and second interlayer dielectric layer, a top

surface portion of said contact pads.

13. The method according to claim 12, wherein said step of etching a top surface portion of said contact pads is performed by one selected from a group consisting of wet etch and dry etch processes so as to remove a conductive stringer between said contact pads.

14. A method for forming a self aligned contact in semiconductor device having a semiconductor substrate, a plurality of conductive structures formed on said semiconductor substrate, and a capping layer coating each of said conductive structures, said method comprising the steps of:

forming an interlayer dielectric layer over said semiconductor substrate and said conductive structures, said interlayer dielectric layer having a planar top surface;

forming a mask pattern over said interlayer dielectric layer, said mask pattern having an opening region including at least two contact regions;

etching said interlayer dielectric layer using said mask pattern, thereby to form a self aligned contact opening exposing a top surface of said semiconductor substrate;

removing said mask pattern;

forming a conductive layer in said self aligned contact opening and over said interlayer dielectric layer; and

planarization-etching said conductive layer and interlayer dielectric layer until a top surface of said capping layer is exposed, thereby to form at least two contact pads.

15. The method according to claim 14, further comprises etching, after said step of planarization-etching said conductive layer and interlayer dielectric layer, a top surface portion of said contact pads.

16. The method according to claim 15, wherein said step of etching a top surface

portion of said contact pads is performed by one selected from a group consisting of wet etch and dry etch processes so as to remove a conductive stringer between said contact pads.

17. A method for forming a self aligned contact in a semiconductor device having a semiconductor substrate, a device isolation layer formed on said semiconductor substrate to define active and inactive regions, and a transistor formed on said active and inactive regions, said transistor being formed of a gate electrode, a gate mask thereon, and a sidewall gate spacer, said method comprising the steps of:

forming an etch stopping layer over said semiconductor substrate and over said transistor;

forming an interlayer dielectric layer over said etch stopping layer, said interlayer dielectric layer having a planar top surface;

forming a mask pattern over said interlayer dielectric layer as to expose said active region and a part of said inactive region, said mask pattern having a T-shaped opening region;

etching said interlayer dielectric layer using said mask pattern until a top surface of said etch stopping layer between said transistor and adjacent transistors is exposed;

removing said mask pattern;

forming a compensation mask layer over said transistor and over said interlayer dielectric layer, said compensation mask layer being deposited a larger amount on a top portion of said transistor and said interlayer dielectric layer than bottom space adjacent to said transistor; and

etching said compensation mask layer and said etch stopping layer until a top surface of said semiconductor substrate adjacent to said transistor is exposed, thereby to form a self aligned contact opening.

18. The method according to claim 17, wherein each of said gate mask, sidewall

gate spacer, and etch stopping layer is made of an insulating material having an etch selectivity ratio to said interlayer dielectric layer.

19. The method according to claim 18, wherein said insulating material is made of one selected from a group consisting of SiN and SiON.

20. The method according to claim 17, wherein each of said gate mask, the gate spacer, and etch stopping layer serves as an etch stopping layer during said step of etching said interlayer dielectric layer.

21. The method according to claim 17, wherein said T-shaped opening region is made of a merged contact region including at least two contact regions.

22. The method according to claim 17, wherein said compensation mask layer is made of one selected from a group consisting of SiN and SiON.

23. The method according to claim 17, wherein said compensation mask layer is provided by such a deposition method that said compensation mask layer has a poor step coverage, said deposition method comprising PECVD method.

24. The method according to claim 17, wherein said compensation mask layer is formed to have a thickness in the range of about 200Å to 1500Å.

25. The method according to claim 17, further comprises forming, after said step of etching the compensation mask layer and said etch stopping layer, forming a conductive layer in said self aligned contact opening and over said interlayer dielectric layer; and planarization-etching said conductive layer and interlayer insulating layer until a top surface

of said compensation mask layer is exposed, thereby to form at least two contact pads.

26. A method for forming a self aligned contact in a semiconductor device, the method substantially as hereinbefore described with reference to any one of Figures 3A to 5E.

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Claims searched: 1-13 & 17-26 **Date of search:** 25 February 1999

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Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.Q): H1K(KHAE,KGAMS,KLECM,KLEXM,KMWA)

Int Cl (Ed.6): H01L 21/768, 21/8242

Other: Online:WPI, JAPIO, EPODOC

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
A	US 5 258 096 (MICRON)	

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